Test Report V2
Single Event Effects (SEE) Testing of the ADG526A
16-Channel Analog Multiplexer

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I. Introduction

The ADG526A is a 16-channel analog multiplexer designed in the advanced LC^2MOS process. This process gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The ADG526A uses 4 binary addresses and 1 enable input, which are all CMOS and TTL compatible, to control the multiplexing. On-chip latches facilitate microprocessor interfacing; the part also features fast switching time, low leakage, and a low on resistance. Another feature of the ADG526A is a break-before-make switching regime which prevents momentary shorting of the input signals. The multiplexer has been tested at NASA Goddard Space Flight Center's Co^{60} Test Facility and Texas A&M University Cyclotron Single Event Effects Test Facility. Five devices were tested for SEE.

II. Devices to Be Tested

The ADG526A devices were designed and fabricated by Analog Devices, Inc. They are fabricated in the advanced LC^2MOS process. All devices were characterized prior to exposure. The five devices tested are from the 0704 Lot Date Code (LDC). Complete package markings for the devices are:

5962-8971001XA
ADG526ATQ/883B
Q 0704 A

Table 1: Packaging information

These are all 28 pin devices in a CerDIP package. The actual devices are shown in the Figure 1.

Product Datasheet: ADG526A.pdf

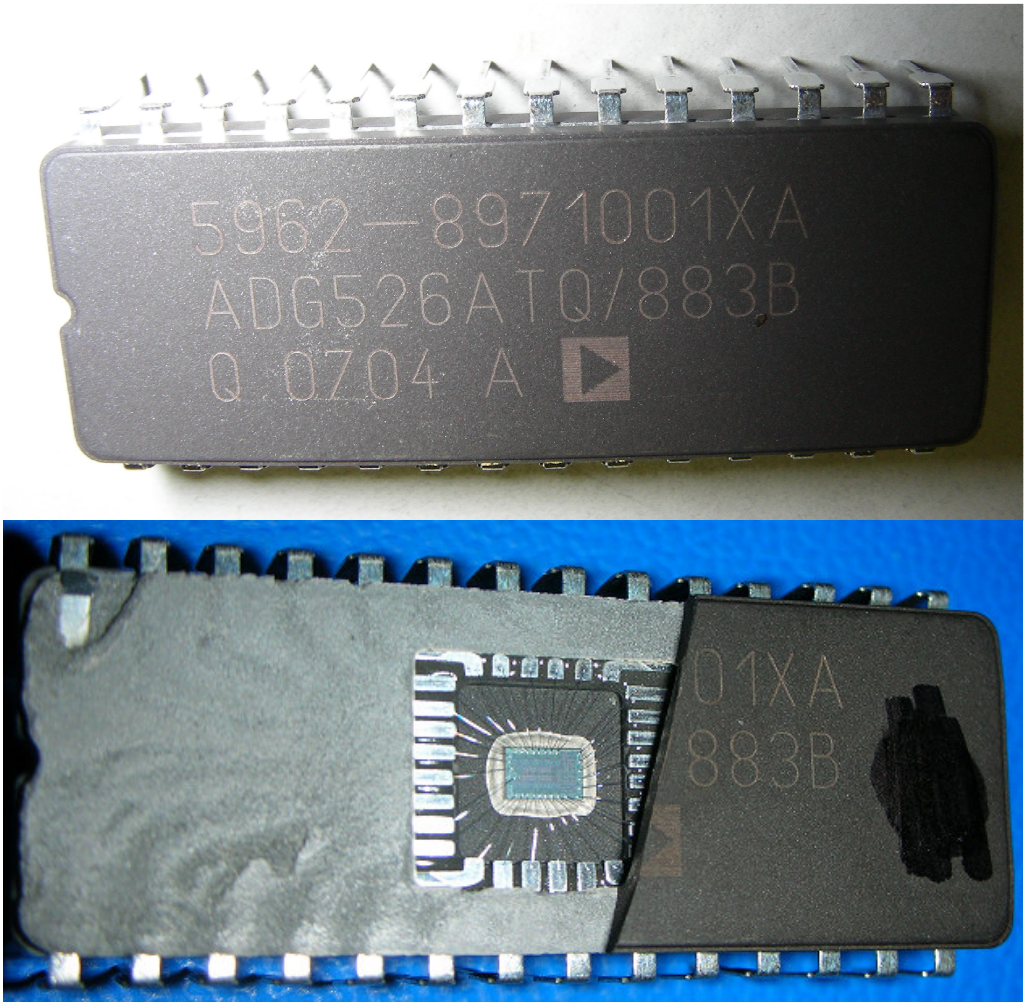

Figure 1: Picture of the ADG526A before (top) and after (bottom) being de-lidded.

III. Test Facility

Facility:
TAMU Cyclotron Single Event Effects Test Facility, using the 15 MeV/amu tune

Total Beam Time:
12 hours

Flux:
5 x 10^2 up to 8 x 10^4 p/cm^2/s

Minimum Fluence Achieved Per Part:
1 x 10^7 p/cm^2

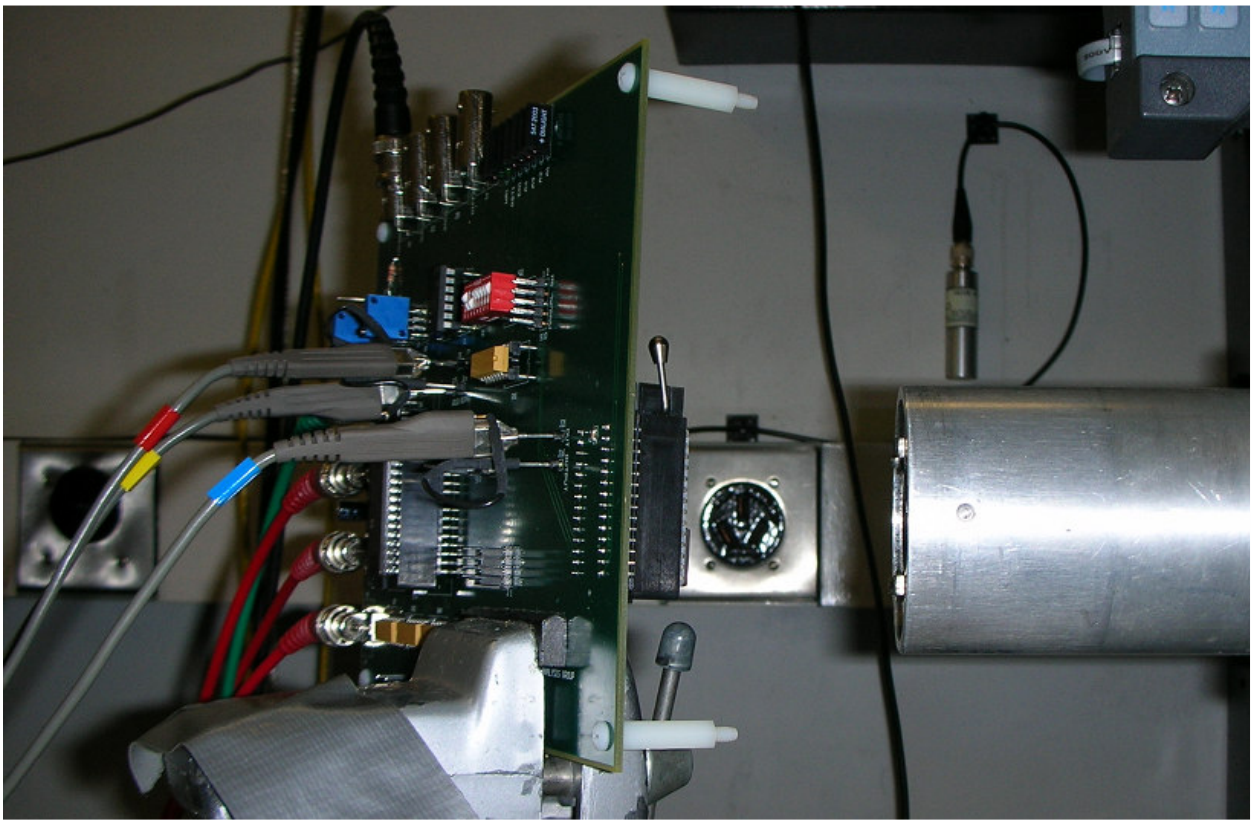

Figure 2: Tester Board and device in the Ion beam at TAMU

Ions used (angle)	LET ($MeVcm^2/mg$)	Range (µm)	Air gap distance from rear foil (cm)
Cu (0)	20.7	117	6.0
Cu (30)	23.9	101	6.0
Cu (45)	29.3	83	6.0
Kr (0)	29.3	116	6.0
Kr (30)	33.8	100	6.0
Kr (45)	41.4	82	6.0
Xe (0)	53.9	102	6.0
Xe (30)	62.2	88	6.0
Xe (45)	76.2	72	6.0
Xe (60)	107.8	51	6.0
Au (0)	87.4	100	6.0
Au (30)	100.9	87	6.0
Au (45)	123.6	71	6.0
Au (60)	174.8	50	6.0

Table 2: TAMU Ion information

IV. Test Methods

Temperature:
Room temperature, 55C, 70C and greater (Latch-up Test)

Test Voltages:
Nominal (15 Volts) supply, 5V digital inputs and 0-5V analog feed through

Operating Speed:
2 kHz

Test Hardware:
The block diagram shown in Figure 2 shows the test setup that was used to test this part for SEE. The Tester Board is used to verify the functionality of each address and the digital controls. This board uses a 5V and +/- 15V power supply, a function generator setup to deliver a rectangular wave @ 2 kHz with a 90% duty cycle (TTL levels), a Universal Counter (HP 5316B), an oscilloscope and multimeter. The multimeter is used to verify the power supply voltages and to set the trigger levels for the window comparator on the Tester Board. The oscilloscope was used to capture the input and output signals for each address, noting any difference in timing or voltage level. The analog inputs are derived from a voltage divider so that each analog input (16 total) is provided with a unique fixed voltage that's greater than 0 volts and less than 5 volts. This produces a "staircase" sawtooth wave at the Analog Mux outputs with each "staircase" step changing every 500 μsec (2 kHz) and the entire "staircase" sawtooth wave repeating every 8 msec (125 Hz). See trace 1 & 2 of Figure 3 showing the DUT output trace and the Gold Reference behind it. Any differences between the DUT and the Gold Reference will be indicated in the "DUT-Gold" trace. The "Trigger" trace will show a pulse whenever a discrepancy (> 250 mVolts) occurs between the DUT & the Gold Reference. The negative-edge of this pulse triggers the oscilloscope to capture the waveforms and also triggers the Universal Counter to count each pulse as it occurs. The "DUT-Gold" & "Trigger" traces were captured during testing but not included in Figure 3 to keep the plots uncluttered for post-analysis of the raw test data.

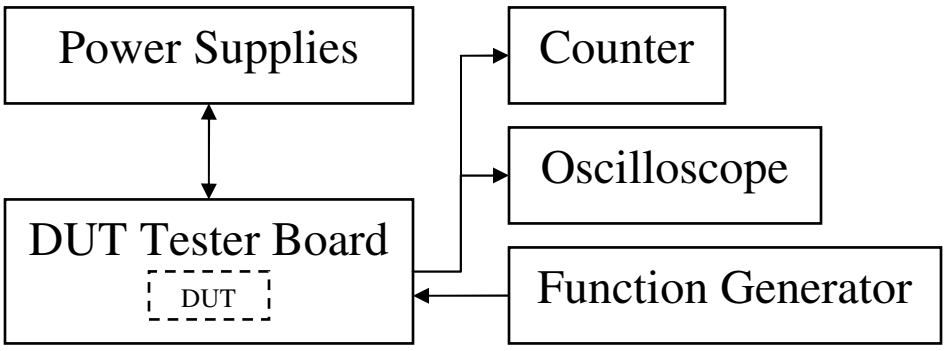

Figure 2: Block diagram of test setup where the dashed line represents the components exposed to the heavy-ion beam.

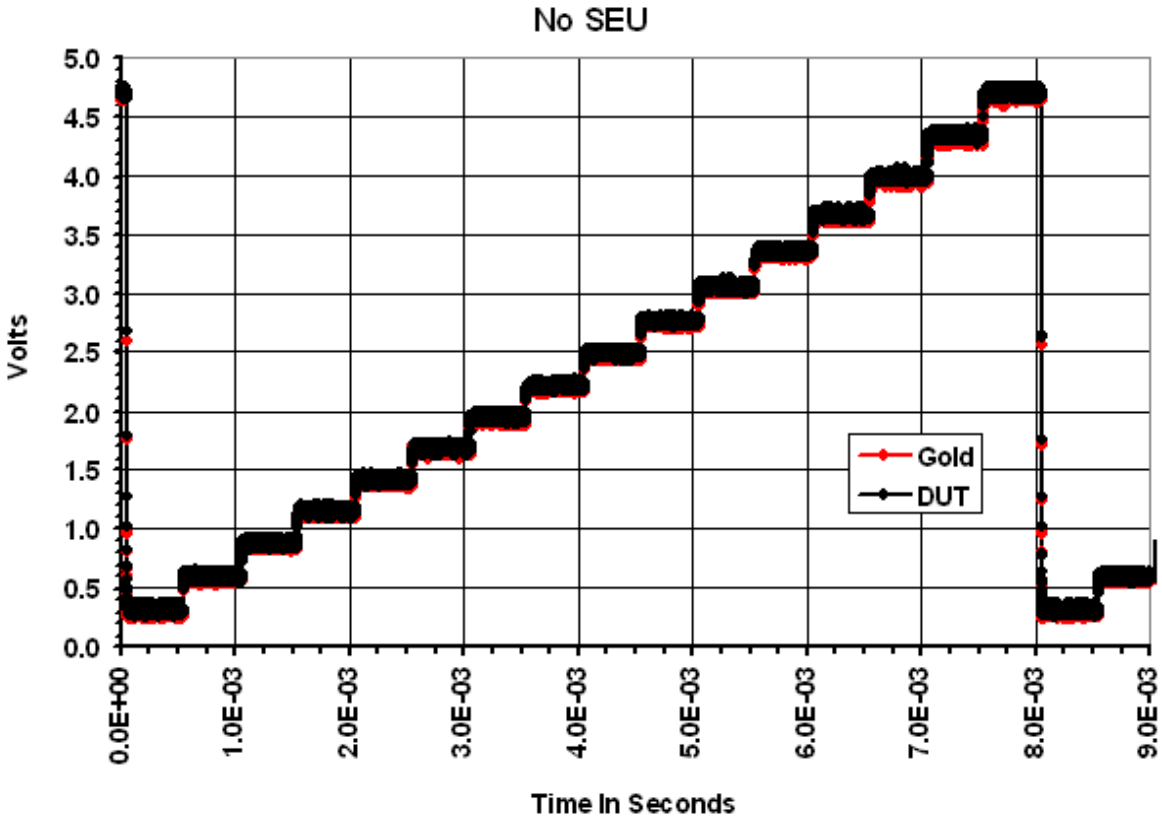

Figure 3: SEE Test – Pass.

The pass test shows a staircase of different voltages for each of the multiplexer channels with no difference on the output and no trigger registered. What this infers is that the DUT and Gold reference chip are in agreement within 250 mV.

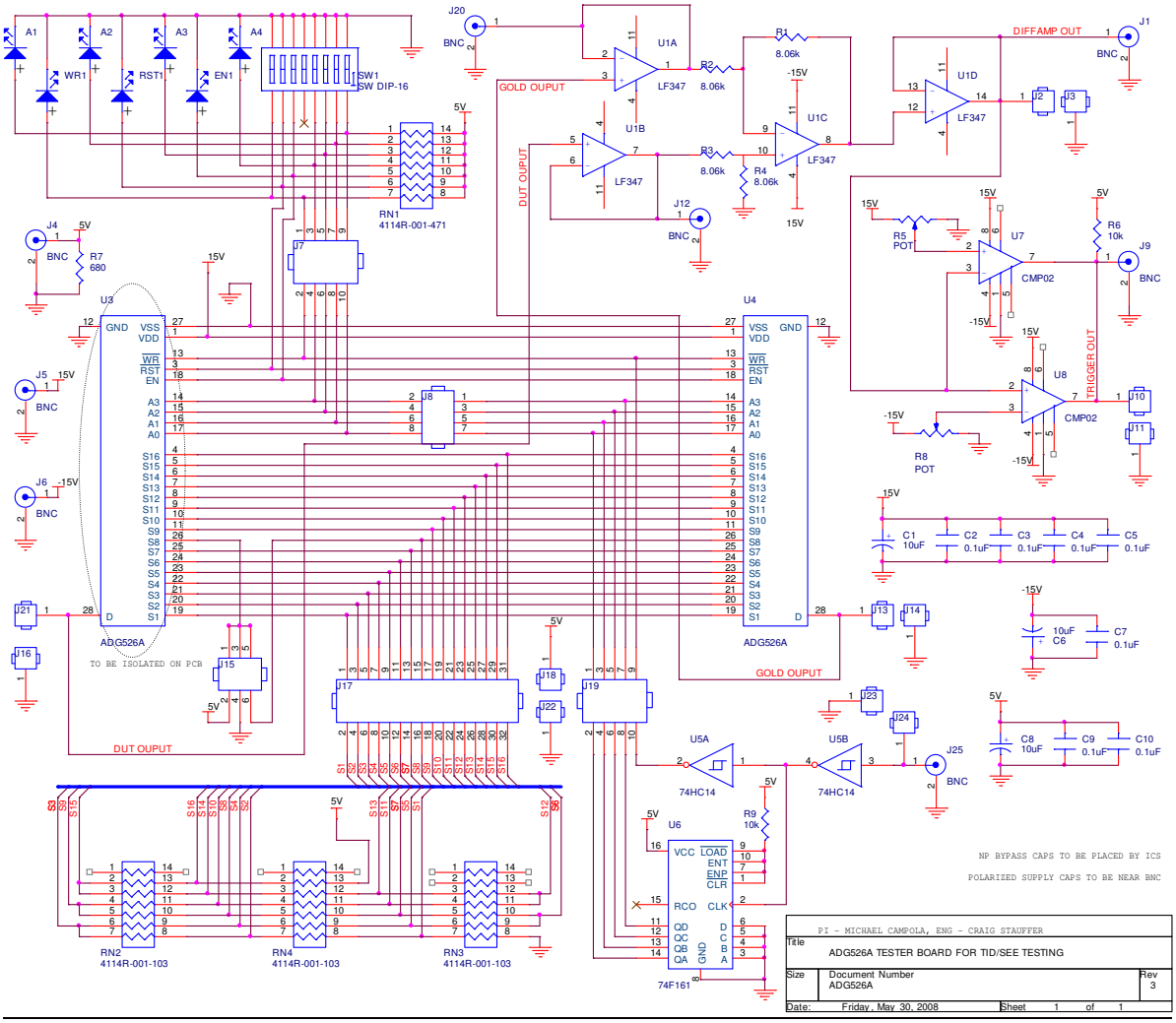

Figure 4: Tester Board Circuit

The schematic above (Figure 4) depicts the tester board circuit that will cycle through all of the addresses autonomously using a counter that runs off of a clock. The DUT output is buffered and then compared to a pristine multiplexer (Gold Reference output) using a difference amplifier with a gain of one. A window comparator provides a pulse that triggers the oscilloscope to capture the waveform & the Universal Counter to increment when the multiplexer outputs do not match within 250 mV. If any address is selected other than the one intended this will register on the trigger, the waveform will show whether the address was stuck or switched to another address, and the test continues. This circuit also allows for individual addresses to be tested if sensitivity is found on a specific address.

The input, DUT output, pristine output (i.e. Gold Reference), difference amplifier output, and the window comparator output (i.e. Trigger) were all monitored during the test. The current on each supply was also monitored for over current conditions.

V. Test Results

Part Failure – No signal output passed, the MUX was incapable of addressing the inputs and connecting to the output. Part failures were found to be dose related, as they reached the limits of TID testing done previously at NASA GSFC, and were not considered due to single events.

Signal Degradation – Input signal is clipped, amplified, or diminishes when passed through the analog MUX, see figures 5, 6, 7 & 8. There were three types of SEU (Single Event Upset) and one type of SET (Single Event Transient) observed during testing:

1. "Latch hit hi", where the output voltage of the ADG526A was that of a higher (binary sequence) address not intended due to an ion hit changing the state of the latched address (i.e. ion hit causes a bit in the address latch to change from a 0 to a 1).
2. "Latch hit lo", where the output voltage of the ADG526A was that of a lower (binary sequence) address that was not intended due to an ion hit changing the state of the latched address (i.e. ion hit causes a bit in the address latch to change from a 1 to a 0).
3. "Float hit", characteristic of an ion strike or accumulated charge on the break-before-make circuitry forcing it to activate which causes no input to be passed and no channel to be connected to the output, hence the floating voltage readings that show an exponential decay from internal/substrate capacitance down to zero volts.
4. "Decoder hit", an ion strike when the device is in latched mode where the address has already been selected and latched and the ion strike did not cause any of the address bits in the latch to change state but instead a very narrow pulse is seen on the output of the DUT that is not present on the pristine output (i.e. Gold Reference) which causes a trigger for the oscilloscope to capture the event and for the HP Universal Counter to increment. This can be considered a SET and is most likely an ion strike on circuitry that is associated with strictly the device output.

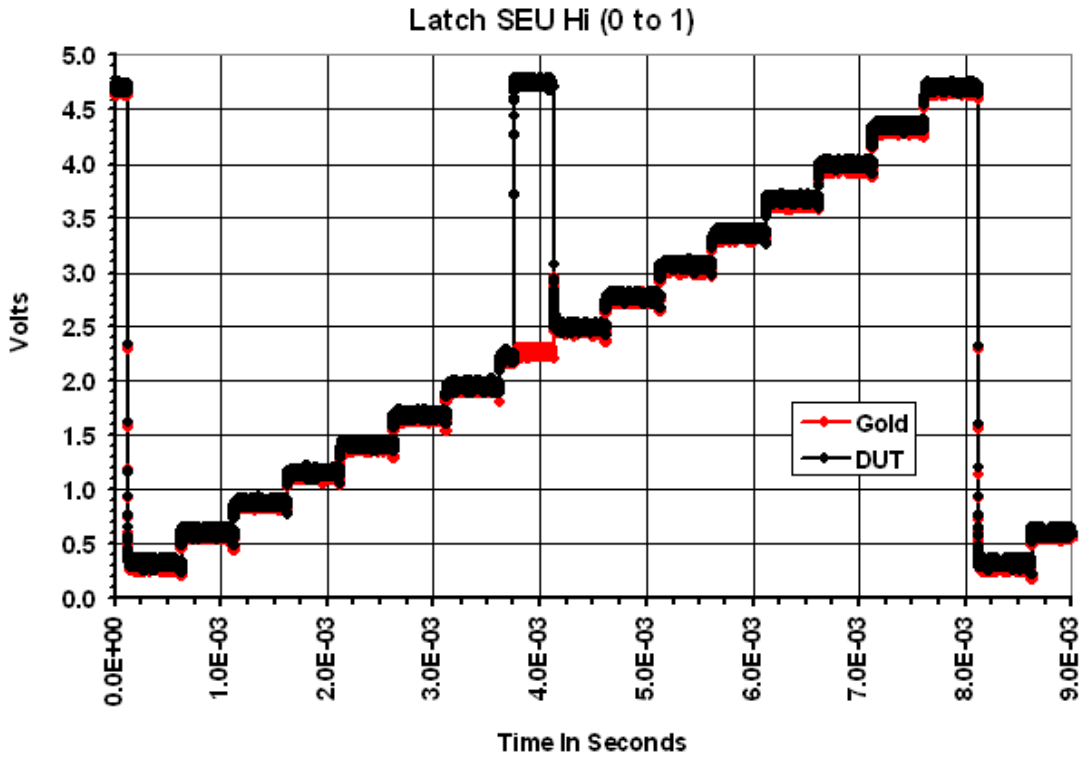

Figure 5: Latch hit hi, SEU where the voltage from an incorrect channel was passed through the analog multiplexer.

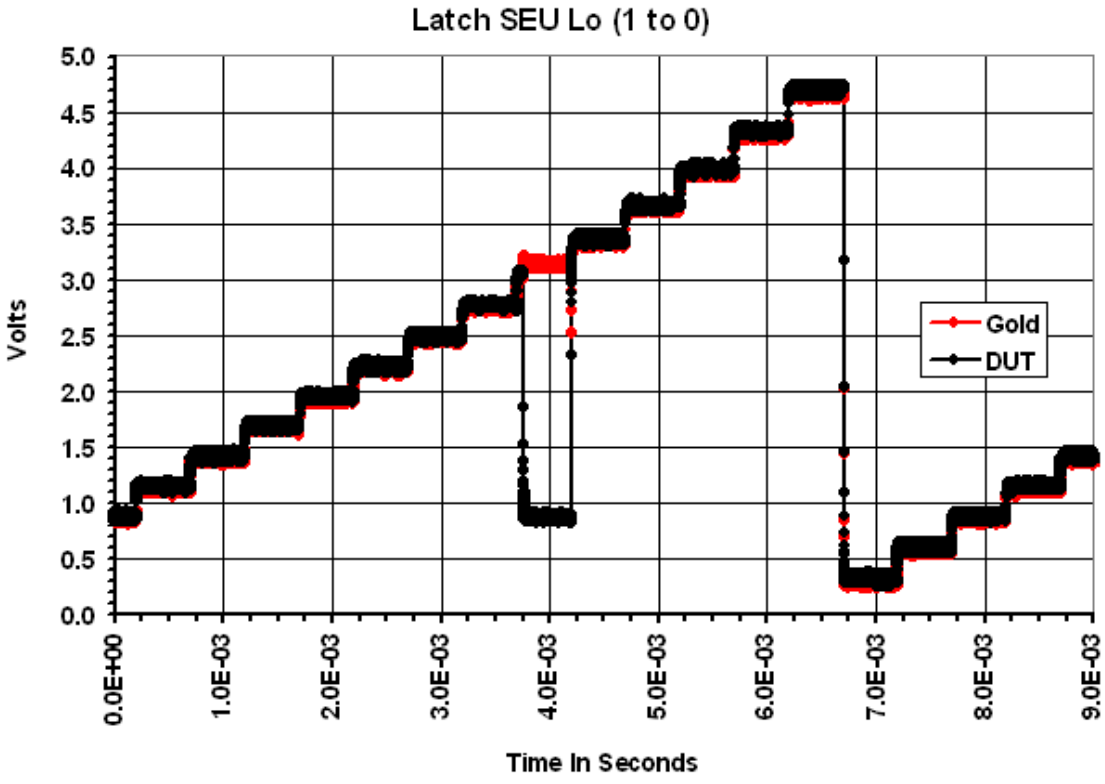

Figure 6: Latch hit lo, SEU where the voltage from an incorrect channel was passed through the analog multiplexer.

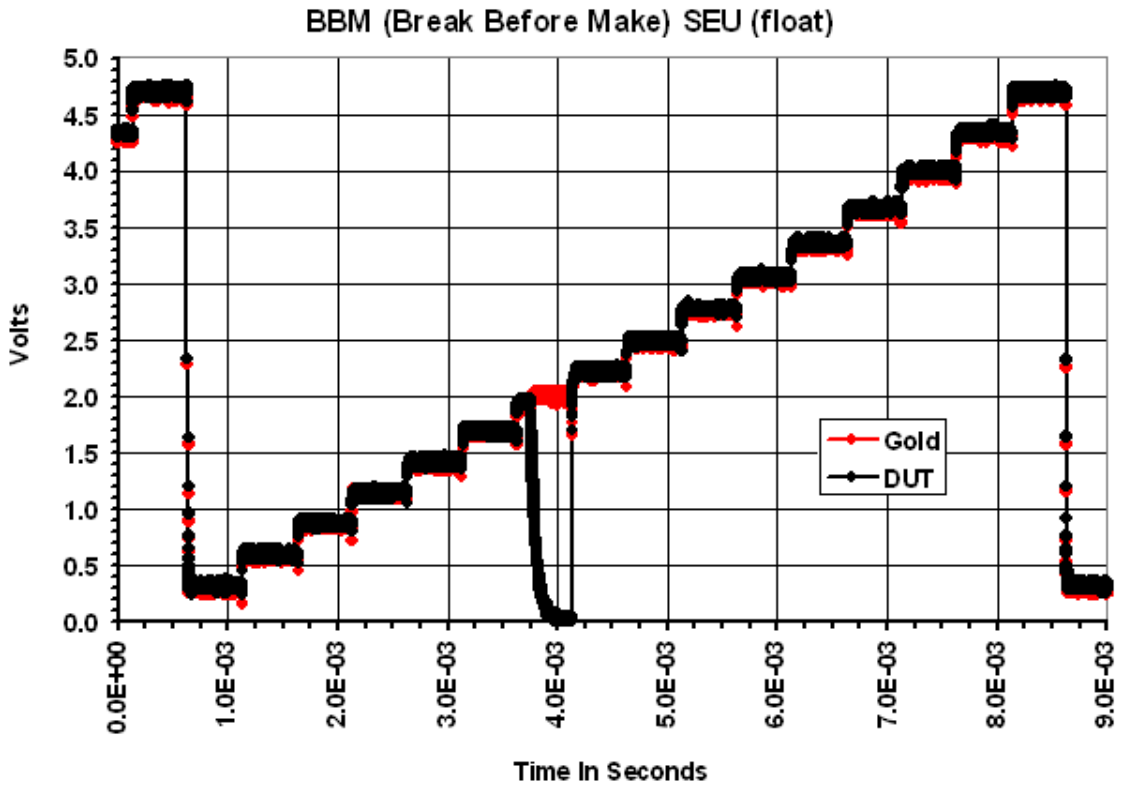

Figure 7: Float hit, SEU where the voltage exponentially decays from selected level to zero.

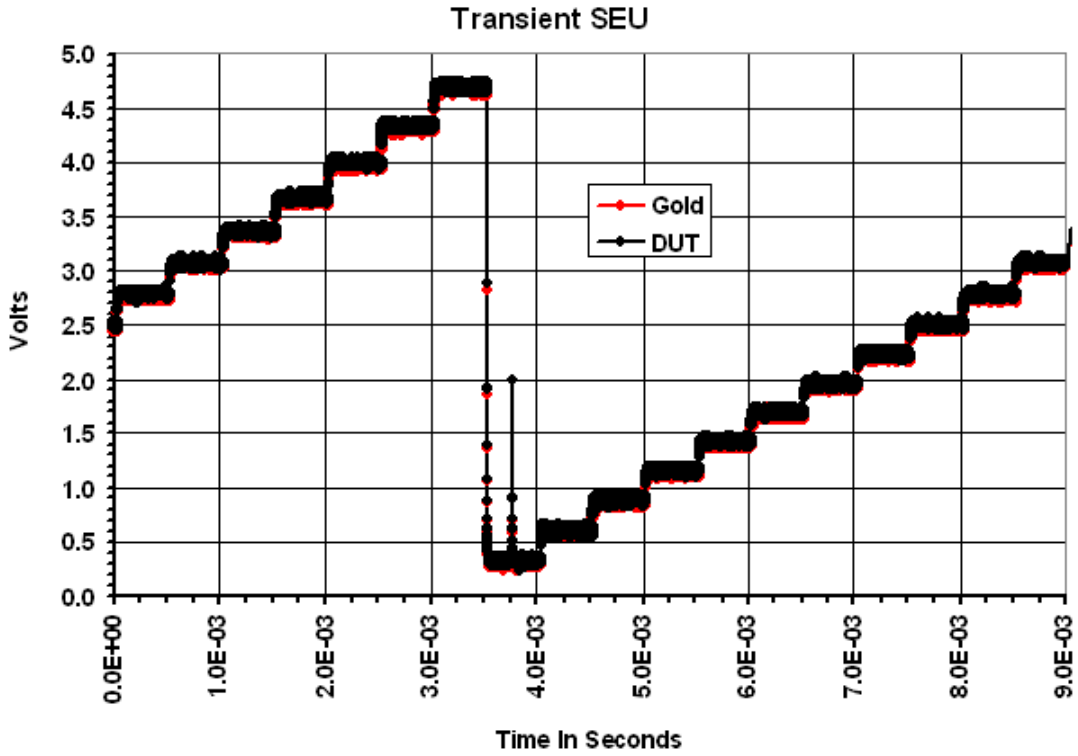

Figure 8: Transient (SET) error recorded while performing SEE testing.

ADG526A Average Cross Section of SEU Events

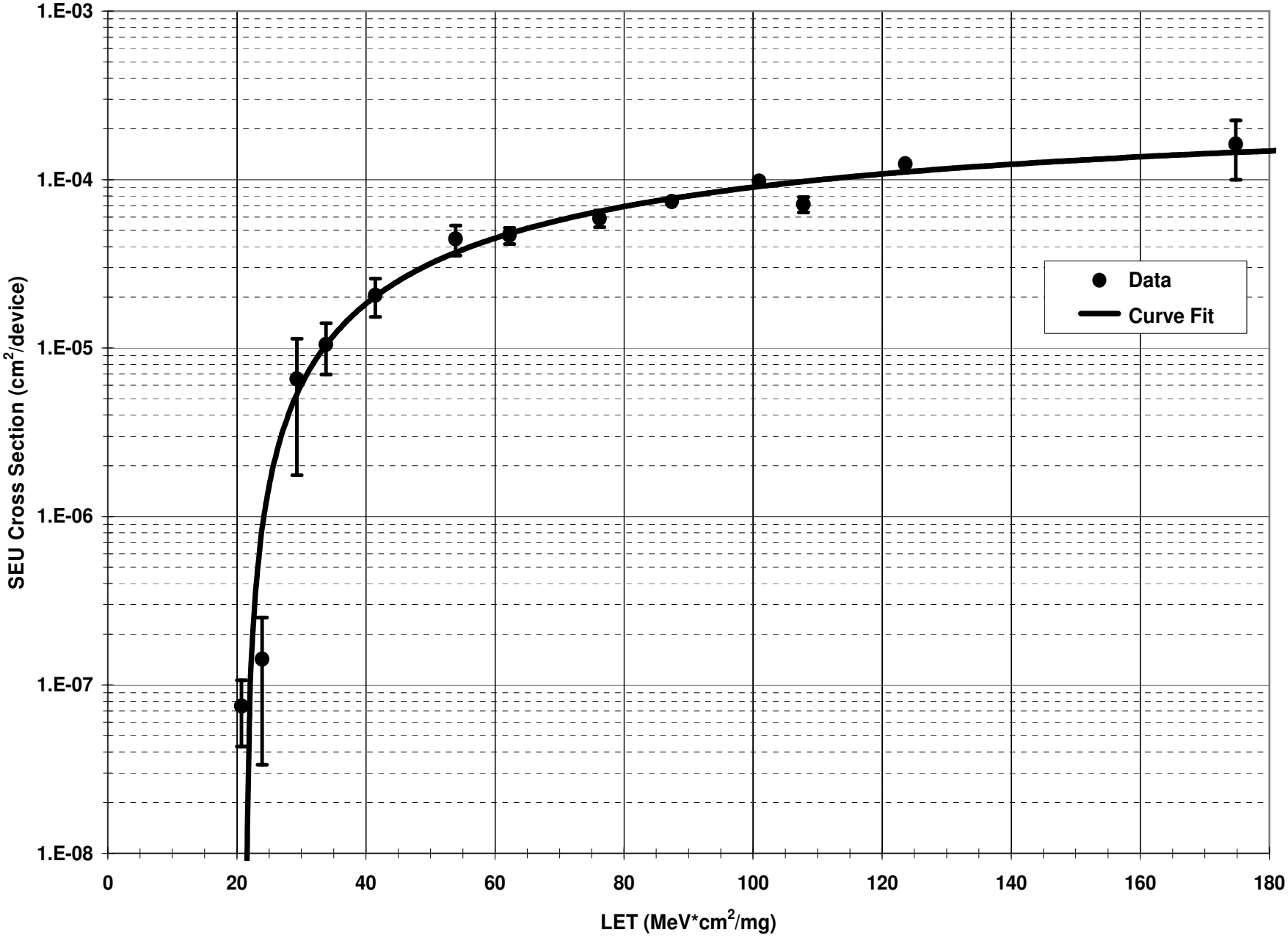

Figure 9: Cross section of the ADG526A device shown with +/- one standard deviation bars at each LET.

VI. Result Synopsis

Five ADG526A parts were tested in the TAMU ion beam; the parts were intermittently tested for LET values of 20.7-to-174.8 (MeV.cm^2/mg) achieving a minimum fluence of 1 x 10^6 (p/cm^2) at each LET per part, to obtain the following results:

Occurrence:	Lowest LET where events were observed:	Highest LET where events were observed:
Latch hit to higher address:	20.7 MeV.cm^2/mg	Observed at all higher LET tested (tested up to 174.8 MeV.cm^2/mg)
Latch hit to lower address:	53.9 MeV.cm^2/mg	Observed at all higher LET tested (tested up to 174.8 MeV.cm^2/mg)
Float hit:	41.4 MeV.cm^2/mg	Observed at all higher LET tested (tested up to 174.8 MeV.cm^2/mg)
SET:	174.8 MeV.cm^2/mg (@80C)	174.8 MeV.cm^2/mg (@80C)
Latch-up Events:	No latch-up events were observed (tested up to 174.8 MeV.cm^2/mg and up to @100C)	No latch-up events were observed (tested up to 174.8 MeV.cm^2/mg and up to @100C)
Multiple bit Latch hits	None observed	None observed

Table 3: LET extremities of events

Part #	Total Fluence (p/cm^2.s)	Total Dose (Rads)	Average Flux (p/cm^2.s)	Test Result
4	4.67E+07	1.95E+04	2.05E+04	still functional
5	1.06E+08	4.64E+04	3.32E+04	dose related failure
6	8.13E+07	2.61E+04	1.81E+04	dose related failure noticed with elevated temperature
7	3.00E+07	2.29E+04	1.18E+04	still functional
9	1.60E+07	2.60E+04	1.01E+04	still functional

Table 4: Results by part.

This part showed a sensitivity to latched address hits from lo to hi addresses (i.e. a latched address bit changing from a 0 to a 1), and at higher LET showed more SEE types. The part did not latch through any of the testing at TAMU, however it showed agreement with TID testing results that led to two part failures on-site due to accumulated dose effects.